What is claimed is:

1. A system for fault injection of a circuit device, comprising:

a fault selection circuit adapted with fault selection data identifying selected circuit outputs of the circuit device,

a fault value circuit adapted with fault values for injection on corresponding selected circuit outputs, and

the fault selection circuit controlling the selected circuit outputs in place of control by system logic during injection of respective fault values.

2. The system as recited in claim 1 wherein, the data and the fault values, respectively, are received from an industry standard, TAP controller.

3. The system as recited in claim 1 wherein, the circuit device comprises a field programmable gate array, FPGA.

4. The system as recited in claim 1 wherein, the circuits are independent of an operating system of the circuit device.

5. The system as recited in claim 1 wherein, the system selects pins for fault injection, and the pins are connected to a circuit board having circuit board interconnections being tested for vector verification by the fault injection values.

6. The system as recited in claim 1 wherein, the system selects pins for fault injection, the pins are connected to a backplane, and the backplane is coupled to a backplane test tool having a backplane test algorithm being tested for verification.

7. The system as recited in claim 1 wherein, the fault selection circuit comprises a user defined scan register in the circuit device.

8. The system as recited in claim 1 wherein, the fault value circuit comprises a user defined scan register in the circuit device.

9. The system as recited in claim 1 wherein, the system selects an internal register for fault injection, and the internal register is in the system logic of the circuit device.

10. A method for injection of fault values at selected fault injection locations of a programmable circuit device, comprising:

storing and updating fault injection selection data in a first register;

scanning and storing fault injection values in a second register; and

updating the fault injection selection data and the fault injection values at the selected fault injection locations of the programmable circuit device, while the selected fault injection locations are controlled by the first and second register instead of by system logic of the circuit device.

11. The method of claim 10, and further comprising;

injecting stuck-on fault injection values on selected pins of the fault injection locations.

12. The method of claim 10, and further comprising:

injecting stuck-at fault injection values on selected pins of the fault injection locations.

13. The method of claim 10, and further comprising:

injecting stuck-on fault injection values on selected pins of the fault injection locations; and

injecting stuck-at fault injection values on selected pins of the fault injection locations.

14. The method of claim 10, and further comprising:

injecting stuck-on fault injection values on selected pins of the fault injection locations while the programmable circuit device is mounted on a circuit board, to test for vector verification of circuitry of the circuit board.

15. The method of claim 10, and further comprising:

injecting stuck-at fault injection values on selected pins of the fault injection locations while the programmable circuit device is mounted on a circuit board, to test for vector verification of circuitry of the circuit board.

16. The method of claim 10, and further comprising:

injecting stuck-on fault injection values on selected first pins of the fault injection locations connected in a fault injection circuit between system logic of the programmable circuit device and the first pins, while the programmable circuit device is mounted on a circuit board, to test for vector routing verification of the circuit board; and

injecting stuck-at fault injection values on selected second pins of the fault injection locations connected in a fault injection circuit between system logic of the programmable circuit device and the second pins, while the programmable circuit device is mounted on a circuit board, to test for vector routing verification of the circuit board.

17. The method of claim 10, and further comprising:

injecting stuck-on fault injection values on selected first pins of the fault injection locations connected in a fault injection circuit between system logic of the programmable circuit device and the first pins, while the programmable circuit device is mounted on a circuit board being tested by verification test software, to test for verification of a new algorithm of the software; and.

injecting stuck-at fault injection values on selected second pins of the fault injection locations connected in a fault injection circuit between system logic of the programmable circuit device and the second pins, while the programmable circuit device is mounted on a circuit board being tested by verification test software, to test for verification of a new algorithm of the software.

18. The method of claim 10, and further comprising: injecting one or more of the fault injection values at an internal register in the system logic of the circuit device.